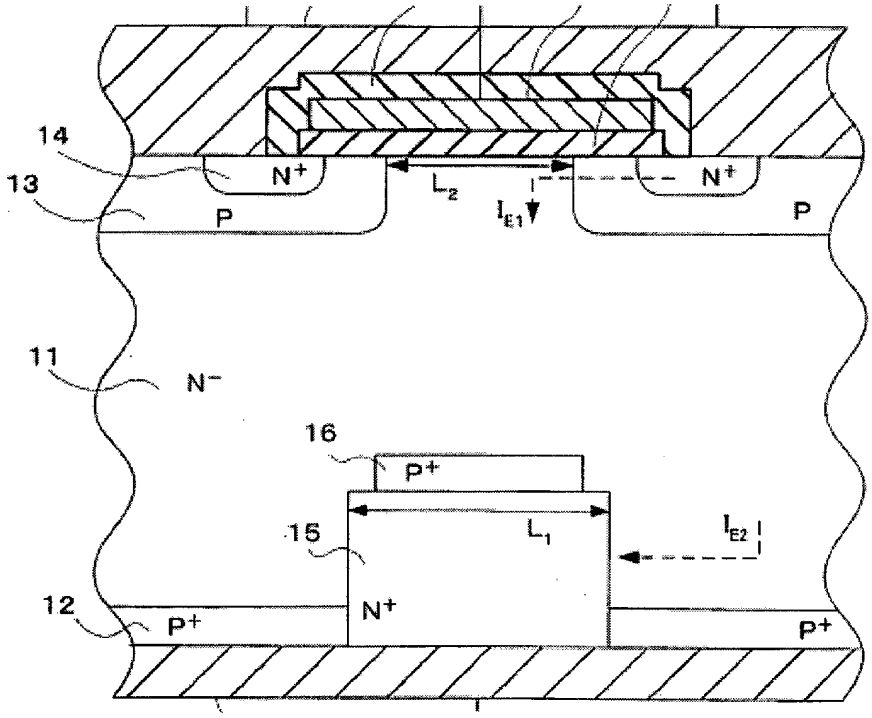
REMARKS/ARGUMENTS

Claims 1-4 and 6-9 are amended by this response. Claim 5 is canceled. Claims 10-11 are added. Upon entry of these amendments and remarks, claims 1-4 and 6-11 will remain pending.

As an initial matter, claims 1-4 and 6-9 are being amended to remove the reference numbers present in the figures.

Embodiments of the present invention relate to a semiconductor device. As shown in FIG. 1 (reproduced below), an embodiment includes a sixth semiconductor region (P+ type semiconductor region 16) formed such that at least a part of a fifth semiconductor region (N+ type collector-short region 15) contacts a first semiconductor region (N- type base region 11):



In this configuration, much of the electron current I_{E1} that flows toward the upper surface of the N+ type collector-short region (15) is blocked by the P+ type semiconductor region (16) to flow along the PN junctions formed by the P+ type collector regions (12) and the N- type base region (11), such that the electron current I_{E2} flows.

Accordingly, the amount of the electron current I_{E1} that flows into the N+ type collector-short region 15 from the upper surface thereof is reduced, and the electron current I_{E2} that flows along the PN junctions formed by the P+ type collector regions 12 and the N- type base region

11 increases. With increasing I_{E2}, the PN junctions are biased deeply in the forward direction to inject holes into the N- type base region 11, thereby producing fine conductance modulation and allowing the semiconductor device to rapidly be turned on and off.

Accordingly, claim 1 has been amended to read as follows:

> 1. An insulated gate semiconductor device, comprising:
> a first semiconductor region having a first conductivity type;
> second semiconductor regions having a second conductivity type, formed in one principal surface of said first semiconductor region;
> third semiconductor regions having the second conductivity type, formed in surface regions of the other principal surface of said first semiconductor region;
> fourth semiconductor regions having the first conductivity type, formed in surface regions of said third semiconductor regions ;
> a first electrode electrically connected to said fourth semiconductor regions;
> a control electrode disposed, via an insulating film, on the other principal surface between said first semiconductor region and said fourth semiconductor regions; and
> a second electrode electrically connected to said second semiconductor regions,
> wherein said insulated gate semiconductor device comprises;
> a fifth semiconductor region having the first conductivity type, formed in the one principal surface of said first semiconductor region so as to be adjacent to said second semiconductor regions; and
> a sixth semiconductor region having the second conductivity type, formed between said fifth semiconductor region and said first semiconductor region, said sixth semiconductor region formed such that at least a part of said fifth semiconductor region contacts said first semiconductor region. (Emphasis added)

Independent claim 9 has been similarly amended.

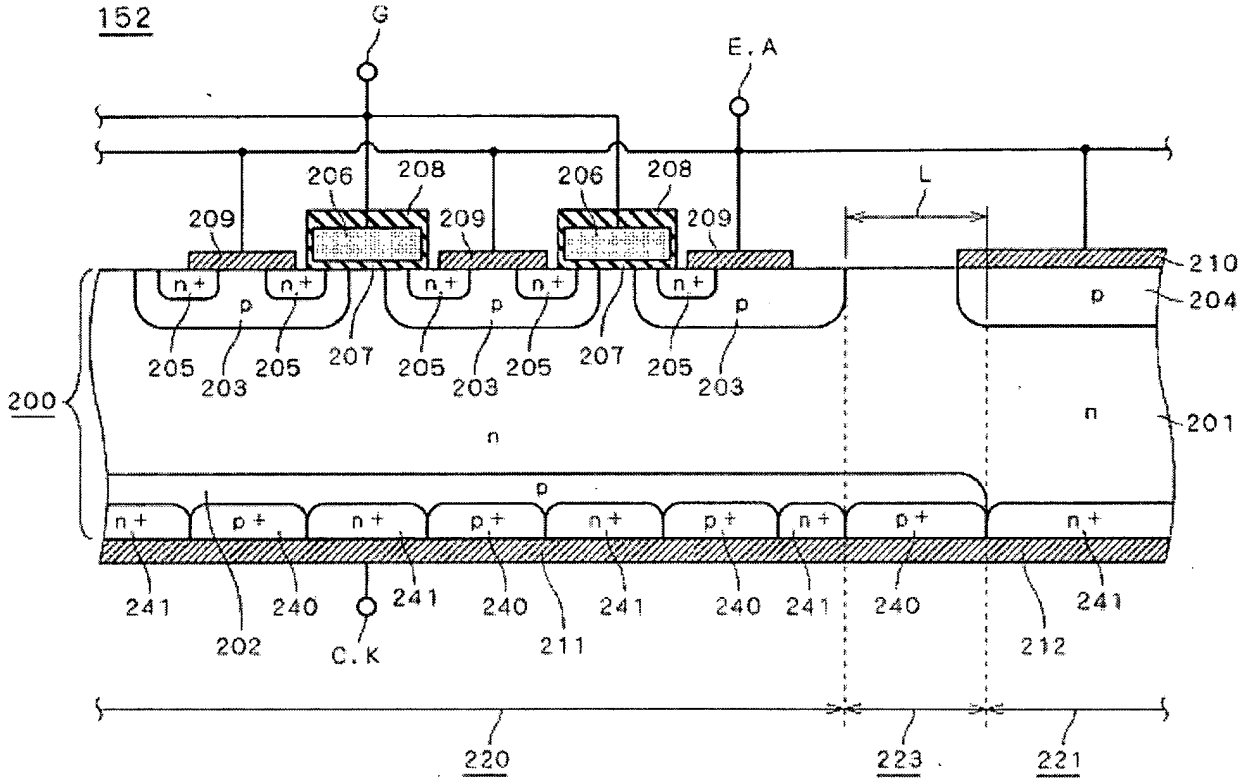
In the latest office action, the Examiner rejected certain claims as anticipated by U.S. Patent Publication No. 2002/0153586 to Majumdar, et al. ("the Majumdar Publication"). These anticipation claim rejections are overcome as follows.

As a threshold matter, the Examiner is respectfully reminded that the claims stand rejected as anticipated, and not merely obvious, in view of the Majumdar Publication:

> for anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. (Emphasis added; MPEP 706.2)

Here, the Majumdar Publication fails to teach, explicitly or impliedly, at least the claimed sixth semiconductor region formed such that at least a part of said fifth semiconductor region contacts said first semiconductor region.

The Examiner cites the conventional device of FIG. 11 (reproduced below) of the Majumdar Publication as disclosing the claimed embodiments:



In particular, the Examiner notes that the n+ type semiconductor region (241) in the right-most region, contacts the region (201).

However, this n+ type semiconductor region (241) is formed in a diode region and all n+ type semiconductor regions of (241) in an IGBT region are covered with the p type semiconductor region (202). Therefore, the Majumdar Publication fails to teach, explicitly or even impliedly, the claimed sixth semiconductor region formed such that at least a part of the fifth semiconductor region contacts a first semiconductor region.

Also in the latest office action, the Examiner rejected certain claims as being anticipated by U.S. Patent No. 5,372,954 to Terashima ("the Terashima Patent"), or by U.S. Patent No. 5,264,378 to Sakurai ("the Sakurai Patent"). Those references, however, also fail to teach

explicitly or even impliedly, at least the claimed sixth semiconductor region formed such that at least a part of said fifth semiconductor region contacts said first semiconductor region.

Specifically, according to the Terashima Patent, the p diffusion region 11 of FIG. 6 is formed to cover the entire n+ diffusion region 12, and the claimed configuration of the first, fifth, and sixth semiconductor regions is not present. As for the Sakurai Patent, collector region 12 of FIG. 6 of that reference, is formed to cover all n+ regions 15, and hence the claimed configuration of first, fifth, and sixth semiconductor regions is again not disclosed.

In view of the failure of the art being relied upon to teach every element of the pending claims, explicitly or even impliedly, it is respectfully asserted that those claims cannot be considered anticipated. Continued maintenance of the anticipation rejections is improper, and these claim rejections should be withdrawn.

Finally, new claims 10-11 are added by this response. Support for these new claims may be found in the specification as originally filed, at least at **¶[0037]**. To avoid any rejection of these new claims 10-11 based upon the art being relied upon by the Examiner, it is respectfully noted that none of the references relied upon by the Examiner teaches a sixth semiconductor region that is formed to be floating.

Specifically, in the Majumdar Publication, the p type semiconductor region 202 is electrically connected to the collector electrode 211 through the p+ type semiconductor regions 240. In the Terashima Patent, the p diffusion region 11 is connected to the collector electrode 9. In the Sakurai Patent, the collector region 12 is connected to the collector electrode 10.

Based upon the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (650) 326-2400 x22223.

Respectfully submitted,

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